Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A1**
2. **B1**
3. **N/C**
4. **C1**
5. **D1**
6. **Y1**
7. **GND**
8. **Y2**
9. **A2**
10. **B2**
11. **N/C**
12. **C2**
13. **D2**
14. **VCC**

**.037”**

**.033”**

**1 14**

**2**

**3**

**4**

**5**

**6**

**13**

**12**

**11**

**10**

**9**

**7 8**

**LS221**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LS21**

**APPROVED BY: DK DIE SIZE .033” X .037” DATE: 6/9/16**

**MFG: MOTOROLA THICKNESS .015” P/N: 54LS21**

**DG 10.1.2**

#### Rev B, 7/1